

## SECTION VII

### TROUBLESHOOTING AND CIRCUIT DIAGRAMS

#### 7-1. INTRODUCTION.

7-2. This section of the manual contains troubleshooting information and circuit diagrams for the Model 3580A Spectrum Analyzer. Included are troubleshooting information, information on factory selected components, functional block diagrams, schematic diagrams and component location diagrams.

#### 7-3. TROUBLESHOOTING AND PREVENTIVE MAINTENANCE.

##### 7-4. General Troubleshooting Procedures.

7-5. Troubleshooting information for the 3580A can be found in the functional block diagrams and circuit diagrams at the end of Section VII. An extensive set of notes, waveforms, and tables has been provided to help narrow the problems down from the functional block, to a board, and finally to a component.

7-6. Use the Overall Functional Block Diagram (Figure 7-1) to narrow the 3580A problem down into one of the four major functional blocks:

- 1) Input Section
- 2) Frequency and Sweep Section
- 3) IF Section
- 4) Display Section.

This diagram gives a good overall look at the 3580A operation. Once the diagram is understood, the failure symptoms alone may be adequate to lead you to the proper block. Other times, the output signals from the 3580A will suffice. For instance, the RECORDER X-AXIS and Y-AXIS outputs give an indication of proper instrument operation up to, but not including, the A7 Logic Board. The TRACKING OSC OUTPUT indicates if the Frequency and Sweep Section is working properly.

7-7. If the external control signals and front panel failure symptoms are not adequate to localize a problem to a particular block, remove the 3580A outer covers and check the appropriate input and output lines of each block. This will localize the problem to a block. The Analog Block Diagram (Figure 7-2), circuit schematics and associated notes can then be used to isolate the problem to the component.

##### 7-8. A2 Board VTO Troubleshooting.

7-9. The A2 VTO is part of a complex feedback loop. If the VTO circuitry is not working properly, the feedback loop can be broken by applying approximately -1.6 V dc to A2TP4. A 0 to +9 V dc signal supplied to the VTO ERROR AMP on the RED jumper lead to the A2 board should then cause the oscillator frequency to vary from 1.0 to 1.5 MHz (0 to 50 kHz Input Frequency). This signal can then be followed around the feedback loop to find the faulty components. Use the waveforms supplied with the A2 board to aid in this process.

##### 7-10. A3 Board Troubleshooting.

7-11. This part of Section VII contains test procedures for the digital control circuitry of the A3 Sweep Board (Schematic 4). If the previous troubleshooting procedures indicate problems with the normal or adaptive sweep circuitry, perform these test procedures.

- a. Position the 3580A front panel controls to:

SWEEP MODE ..... REP

Short A3TP1 to the gray jumper wire connected near the center of the A3 board (Don't remove the gray jumper).

- b. Adjust A3R54 (INTEGRATOR BALANCE) to verify that the output of the Ramp Integrator (A3TP1) can be adjusted from a positive to negative dc voltage. Readjust A3R54 for 0.000 volts  $\pm$  .001 volts.

- c. Measure  $V_{gs}$  on the dual FET, A3Q1. Both FET's should have  $V_{gs} \leq 3$  V dc.

- d. Set switch S1 to the test position (UP position). Verify that CLOCK OUTPUT (A3U8 pin 11) is a TTL HIGH ( $\geq 2.0$  V dc). Return S1 to the normal position.

- e. Remove the clock test jumper between Q18 and S1. Reposition:

SWEEP MODE ..... RESET

- f. Connect a logic clip to A3U5. Turn the 3580A POWER switch OFF then back to ON. The instrument should come up in state 000 or 100, where the C, B, and A state outputs are located on pins 13, 14 and 15 respectively of A3U5. If the instrument comes up in state 000, clock it to state 100 by momentarily switching A3S1 into, and then out of the test position. (This process will be called "clocking S1" from now on.)

- g. Reposition the following front panel controls:

ADAPTIVE SWEEP ..... OFF  
 RESOLUTION BANDWIDTH ..... 100 Hz  
 FREQ. SPAN/DIV ..... 2 KHz  
 SWEEP TIME/DIV ..... .1 SEC/DIV

- h. Check the following:

1. Collector of A3Q4: 10 volts  $\pm$  .1 volts
2. Collector of A3Q16: 0.0 volts  $\pm$  .1 volts
3. A3U5 pin 5: TTL LOW (as measured by logic clip).
4. A3U5 pins 2, 3, 4, 6 and 9: TTL HIGH (as measured by logic clip).
5. A3TP2: -.25 volts  $\pm$  .02 volts.
6. A3TP3: +.175 volts  $\pm$  .02 volts.
7. A3U8 pin 6: TTL HIGH ( $>$  2.0 volts).

- i. Manually "clock" S1 once and verify that the state does not change from 100.

- j. Short A3TP3 to A3TP4. Verify that the voltage at A3TP11 can be changed from a negative to positive voltage by rotating A3R14. Readjust A3R14 so the voltage at TP11 is at the 0 V transition point. (In some cases it will alternate between positive and negative.)

- k. Check for proper source voltage on A3Q14.  
 (.1  $<$   $V_s$   $<$  +4).

- l. Readjust A3R14\* fully CCW. Reposition:

ADAPTIVE SWEEP ..... CW

- m. (L)RESP (A3U7 pin 5) should be a TTL HIGH. Verify that any one of the following will cause (L)RESP to go LOW.

ADAPTIVE SWEEP ..... CCW  
 SWEEP TIME/DIV ..... .05 SEC/DIV  
 or faster

If (L)RESP doesn't function properly, check the A8 board.

- n. In the following tests, the proper next state qualifiers are set up and the control logic is manually stepped to the next state by "clocking" S1 once. In each case the control logic should go to the next state only when all qualifiers are met and S1 is clocked.

- o. If the control logic fails to clock to the proper state, reset the logic to state 000 or 001 by selecting:

SWEEP MODE ..... RESET

and momentarily turning the POWER switch OFF and then back to ON. Use Table 7-1 to reclock the control logic up to that state which will not go to the proper next state after clocking S1. Then recheck all the next state qualifiers, as given in Table 7-1 and test for proper inputs to the state flip-flops (U6 and U7). The J and K inputs to these flip-flops should correspond to the change the flip-flop will make on the next clock pulse. For instance, if a flip-flop's Q-output is to change from a 0 to a 1, its J input should be high. Likewise, if it is to change from a 1 to a 0, the K input should be high. If it is to stay at 1, the K input should be a 0. If it is to stay at 0, the J input should be a 0.

**Table 7-1. Conditions for Single Stepping A3 Logic.**

(Initial Setup: [Gray Jumper - TP1], [TP3 - TP4], A3R14\* fully CCW, ADAPTIVE SWEEP - OFF, 100 Hz Bandwidth, 2 kHz/DIV, .1 SEC/DIV, RESET.)

Present State	Next State	Conditions to go to next State	Next State Qualifiers
CBA 0 000	CBA 1 100	SWEEP MODE: RESET	(L)SING - HIGH and (H)GEW - HIGH or (L)RESET - LOW
1 100	2 101	SWEEP MODE: SING	(H)DLYO - HIGH (L)RESET - HIGH
2 101	3 111	ADAP. SWEEP: CW	(L)RESP - HIGH
3 111	4 110	R14: CW*	CCMP - HIGH (L)RESP - HIGH
4 110	5 010	ADAP. SWEEP: CCW	(L)RESET LOW
5 010	6 011	R14: CCW*	CCMP - LOW
6 011	7 001	(Clock after delay)	(H)DLYO - HIGH
7 001	2 101	R14: CW*	CCMP - HIGH

\*If A3R14 has a black casing, set it opposite to the setting given.

See Table 7-2. Notice also that the J and K inputs are not directly accessible on U7. All the inputs to each of the input AND gates must be high before there is a corresponding HIGH level given to one of the internal J or K inputs of the flip-flop.

**Table 7-2. Excitation Table for J – K Flip-Flop.**

$Q_t$ (Before Clock)	$Q_t + 1$ (After Clock)	J	K
0	1	1	don't care
1	0	don't care	1
1	1	don't care	0
0	0	0	don't care

p. Reposition (Only those controls printed in **BOLD** require a change from the previous tests.)

**ADAPTIVE SWEEP** ..... **OFF**  
**RESOLUTION BANDWIDTH** ..... 100 Hz  
**FREQ. SPAN/DIV** ..... 2 KHz  
**SWEEP TIME/DIV** ..... **0.1 SEC**  
**SWEEP MODE** ..... **RESET**  
**A3R14** ..... fully CCW\*

q. State 100

1. Clock S1, observe no change of state.
2. Check the voltage at A3TP5 and A3TP6, it should be 0 V dc  $\pm$  .1 V.
3. Short the A3 gray jumper to A3TP1 and short A3TP3 to A3TP4 if not already done.

4. Reposition:

**SWEEP MODE** ..... **SING**

5. Clock S1, and the logic should go to State 101.

r. State 101

1. Clock S1 and observe no change of state.
2. Check for the following levels:

Collector A3Q4 : < - 8 V dc  
 Collector A3Q16: 0 V dc  $\pm$  .1 V  
 A3TP5: < - 7 V dc  
 A3TP6: 0 V dc  $\pm$  .1 V  
 A3TP8: TTL LOW (< .8 Vdc)

3. Reposition:

**ADAPTIVE SWEEP** ..... **CW**

4. Clock S1 once, and the logic should go to State 111.

s. State 111

1. Adjust A3R14 fully CCW\*.
2. Clock S1 and observe no change of state.
3. Check for the following levels:

Collector A3Q16: -9.9 V  $\pm$  .1 V  
 A3TP5: < - 7 V  
 A3TP8: TTL LOW (< .8 V)

4. Reposition:

**ADAPTIVE SWEEP** ..... **CCW**

Clock S1 and observe no change of state.

5. Adjust A3R14 fully CCW.  
Clock S1 and observe no change of state.

6. Reposition:

**ADAPTIVE SWEEP** ..... **CW\***

Adjust A3R14 fully CCW\*.  
Clock S1 and observe no change of state.

7. Adjust A3R14 fully CW\*. Clock S1, and the logic should go to state 110.

t. State 110

1. Clock S1 and observe no change of state.
2. Remove the test lead between A3TP3 and A3TP4. The voltage at A3TP3 should be - .25 V  $\pm$  .1 V.  
Replace the jumper.

3. Check the following levels:

A3TP6: < - 6 V  
 A3TP5: 0 V dc  $\pm$  .1 V  
 Collector of A3Q16: 0 V  $\pm$  .1 V.

4. Adjust R14 fully CCW\*.  
Clock S1 and observe no change of state.

5. Reposition:

**ADAPTIVE SWEEP** ..... **CCW**

Adjust R14 fully CW\*.

6. Clock S1, and the logic should go to state 010.

u. State 010

1. Clock S1 and observe no change of state.
2. Check for the following levels:

\*If A3R14 has a black casing, set it opposite to the setting given.

A3TP6:  $> +6\text{ V}$   
 A3TP5:  $0\text{ V} \pm .1\text{ V}$   
 A3TP8:  $+9.5\text{ V} \pm .5\text{ V}$   
 Collector A3Q16:  $-9.9\text{ V} \pm .1\text{ V}$

3. Reposition:

RESOLUTION BANDWIDTH ..... 1 Hz

4. Connect an oscilloscope to the collector of A3Q11. Wait 5 seconds. The voltage should be a TTL HIGH ( $\geq 2\text{ V dc}$ ).
5. Adjust A3R14 fully CCW\*.
6. While watching the oscilloscope clock S1. The oscilloscope should indicate a TTL LOW ( $< .8\text{ V}$ ) for a few seconds and then return HIGH. The logic state should be 011.

v. State 011

1. Check the following levels:

A3TP5:  $0\text{ V dc} \pm .1\text{ V}$   
 A3TP6:  $0\text{ V dc} \pm .1\text{ V}$   
 Collector of A3Q16:  $-9.9\text{ V} \pm .1\text{ V}$   
 A3TP8: TTL LOW ( $< .8\text{ V}$ )

2. Reposition:

RESOLUTION BANDWIDTH ... 100 Hz

3. Clock S1 and the control logic should go to state 001.

w. State 001

1. Clock S1 and observe no change of state.
2. Check the following levels:

Collector A3Q16:  $-9.9\text{ V} \pm .1\text{ V}$   
 A3TP5:  $< -7\text{ V}$   
 A3TP8: TTL LOW ( $< .8\text{ V}$ )

3. Adjust A3R14 fully CW\*. Clock S1, and the control logic should go to State 101.

x. Adjust R14 so that the voltage at A3TP11 is at the transition between a plus and minus voltage.

y. Remove all test leads and replace the clock jumper. The 3580A should sweep normally. The penlift relay should "click" in single sweep mode and the output of the A3 RAMP GENERATOR (A3TP1) should be  $+5\text{ volts}$  nominal for a front panel display indication at the right graticule. If the LOG SWEEP mode will not work, see the A3 schematic notes.

## 7-12. A7 Board.

7-13. The A7 Board (03580-66507) is available as a rebuilt exchange board (03580-69507) through your local -hp- Sales and Service Office. Many times, however, the board can be repaired without purchasing an exchange board. The following procedure will aid in determining whether the A7 board or the analog circuits preceeding the A7 board are at fault.

a. Connect the 3580A X-AXIS output on the rear panel to the X deflection EXT INPUT of an oscilloscope. A scope with variable persistence works best but is not absolutely necessary. Connect the 3580A Y-AXIS output to the vertical input of the scope. This procedure effectively half splits the 3580A for troubleshooting purposes.

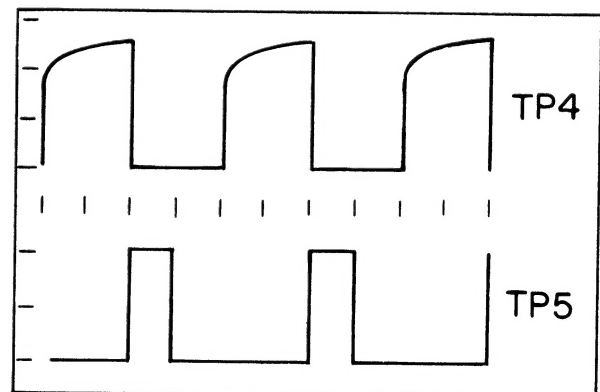
1. If the signal seen of the scope is correct and the signal seen on the 3580A display is incorrect then the problem is in the A7, A8, or A13 boards. If the signal seen on the scope is incorrect DO NOT troubleshoot the A7 board until repairs are made to preceeding circuitry. (See Functional Block Diagram in the Operating and Service Manual.)
2. If the scope presentation is good but the 3580A display is incorrect, check A7TP1. If the presentation is bad there then troubleshoot the A7 board, otherwise troubleshoot A8 or A13.

## 7-14. Troubleshooting the A7 board.

a. Check A7Q2, Q4, Q6, Q8, and Q9. If these parts are P/N 1853-0098 replace all 5 of them with P/N 1853-0010. The new type is much more reliable and is being used in all instruments with serial numbers above 1415A01276.

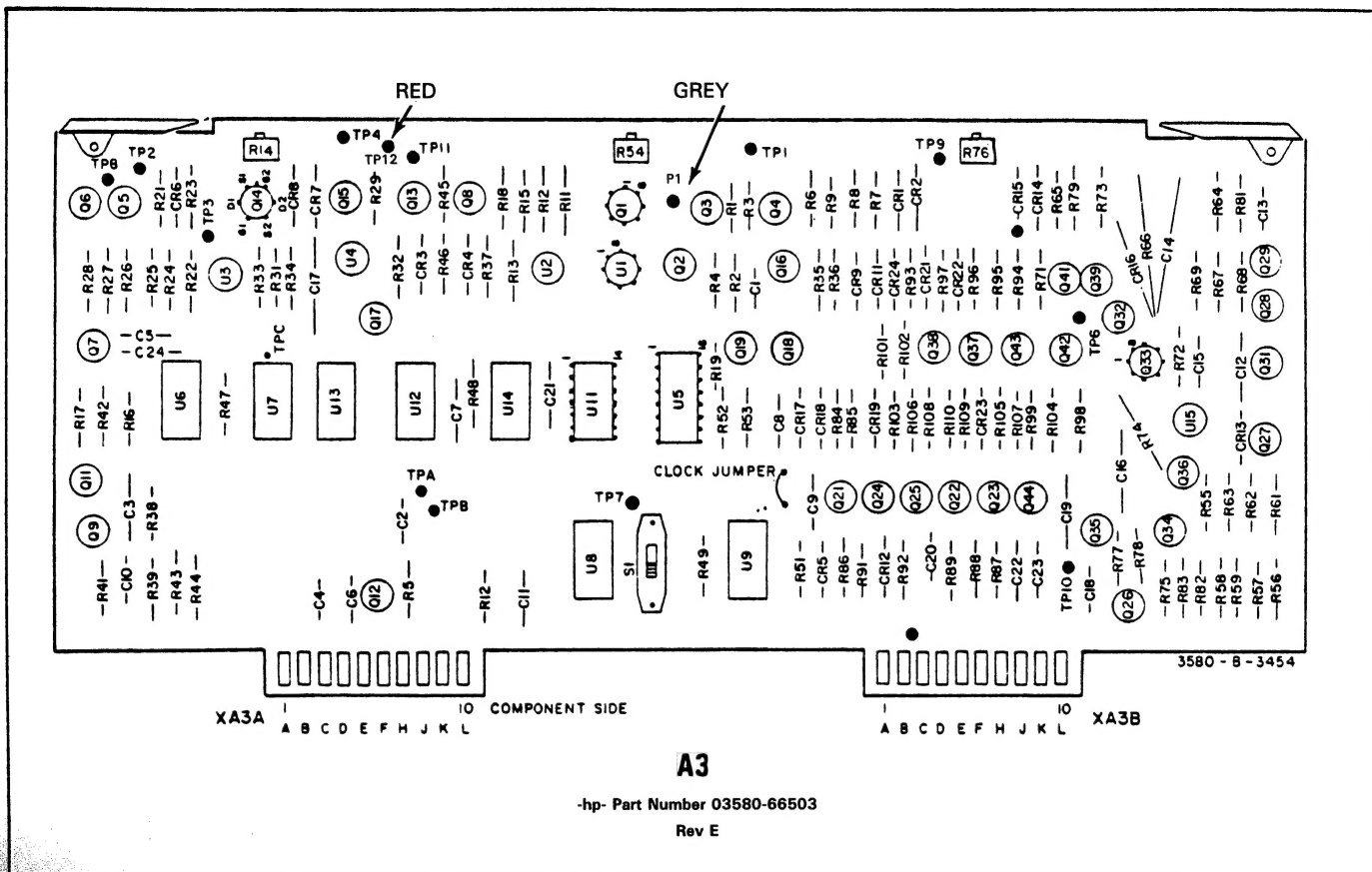
b. Check A7TP4 and A7TP5. They should look similar to the figure shown below.

Horiz  $2\text{ }\mu\text{ sec/div}$   
 Vert  $.2\text{ V/div}$  (with 10:1 probe)



The frequency must be 55 K - 70 kHz! If the frequency is off check A8TP9. The clock frequency is determined by the A8 board.

\*If A3R14 has a black casing, set it opposite to the setting given.

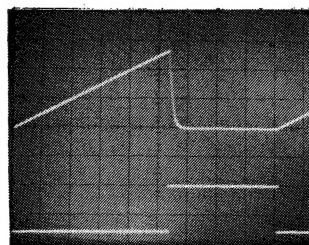


3580A

ADAPTIVE SWEEP .....OFF  
 DISPLAY ..... All pushbuttons released  
 FREQUENCY ..... 00.0 kHz  
 START - CTR .....START  
 DISPLAY SMOOTHING ..... MIN  
 RESOLUTION BANDWIDTH .....300 Hz  
 FREQ. SPAN/DIV .....5 KHz  
 SWEEP TIME/DIV ..... 0.01 SEC  
 SWEEP MODE ..... REP

#### OSCILLOSCOPE

DC coupled, dual trace (chopped), triggered by Channel B.



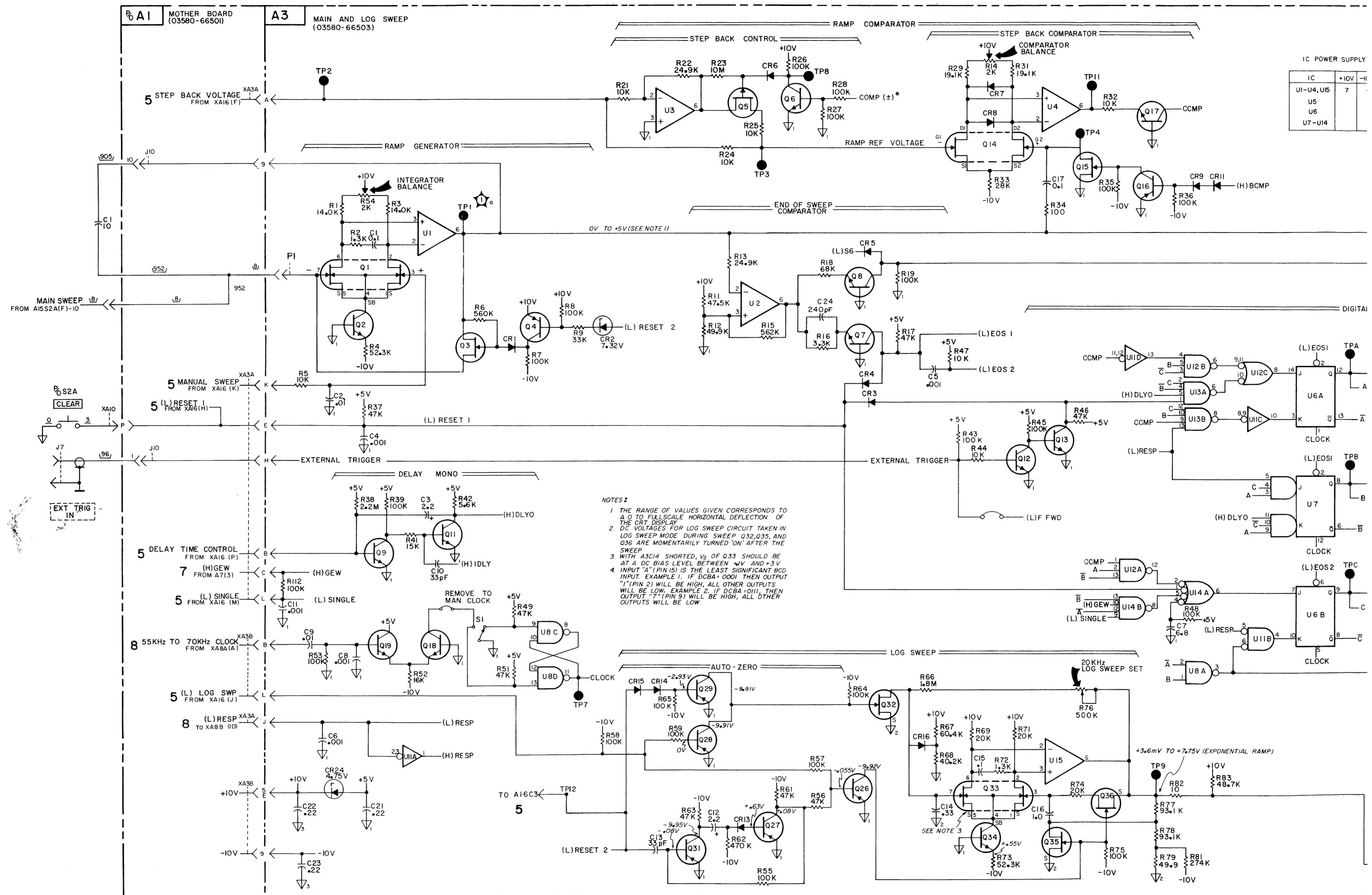
Chan A  
 .2V/div.

←0V

←0V  
 Chan B  
 .5V/div.

20msec/div

A 10:1 divider probe was used on the oscilloscope input. The vertical amplitude sensitivity is the actual amplifier setting and does not reflect the X10 multiplier introduced by the probe.



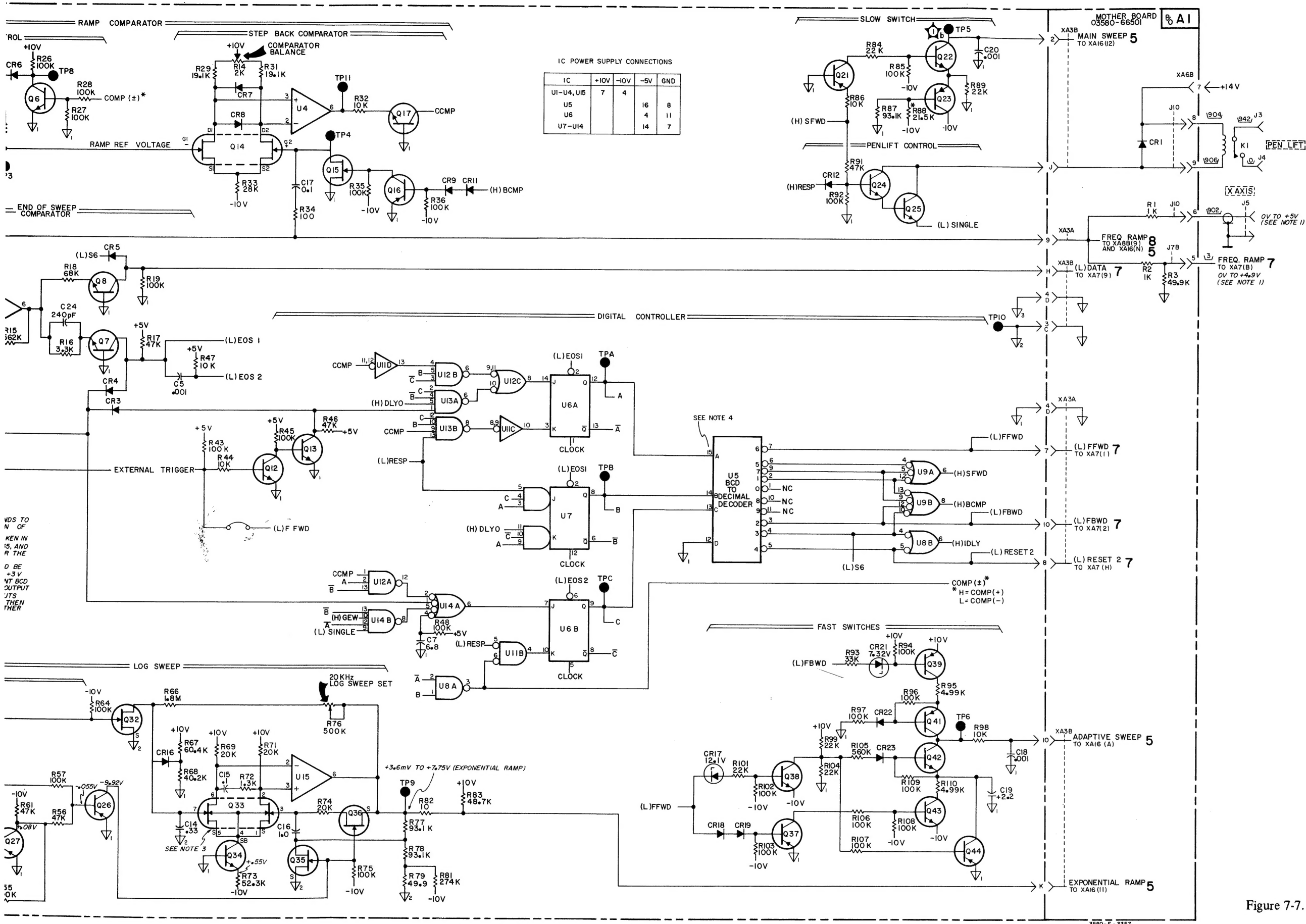
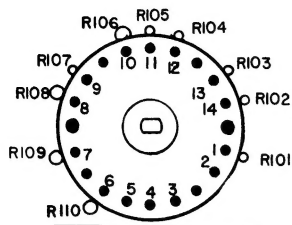


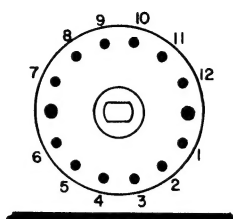
Figure 7-7. Sweep Generator (A3) Schematic and Component Location Diagram.



RESISTORS MOUNTED  
BETWEEN WAFERS  
B & C ON SI.



FRONT VIEW  
PIN POSITIONS FOR  
A14SI



FRONT VIEW  
PIN POSITIONS FOR  
A14S2  
A15SI  
A15S2

